information;

storing the parasitic information in an accessible format; and

running a curve-fitting engine to create the wire load model, wherein running the

curve-fitting engine is dependent on the parasitic information.

11.	(Amended) A computer system, comprising:

a memory for storing a model of a circuit;

a processor for creating a wire load model, wherein the processor establishes an interconnect configuration for the circuit;

a field solver for determining parasitic information for the interconnect configuration, wherein the parasitic information comprises capacitance and resistance information; and

a curve-fitting engine that uses the parasitic information to generate the wire load model.

12.	(Amended) The [method]computer system of claim 11, wherein a width and a spacing for the interconnect configuration is chosen so that the width and spacing is larger than a minimum width and spacing specification for the interconnect configuration.

13.	(Amended) The [method]computer system of claim 11, wherein the curve-fitting engine is a non-linear curve-fitting engine.

14.	(Amended) The [method]computer system of claim 11, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

15.	(Amended) A method for creating a wire load model, comprising:

creating an interconnect configuration;

generating parasitic information for the interconnect configuration, wherein the

parasitic information comprises capacitance and resistance information;